JPL NO. 9950-551

DRL Line Item No. 9

DOE/JPL-955825-81/1
Distribution Category UC 63

EVALUATION AND VERIFICATION OF EPITAXIAL PROCESS SEQUENCE FOR SILICON SOLAR-CELL PRODUCTION

D. Redfield
RCA Laboratories
Princeton, New Jersey 08540

QUARTERLY REPORT NO. 1

APRIL 1981

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, under NASA Contract NAS7-100 for the Department of Energy.

The JPL Low-Cost Silicon Solar Array Project is funded by DOE and forms part of the DOE Photovoltaic Conversion Program to initiate a major effort toward the development of low cost solar arrays.

Prepared under Contract No. 955825 for

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
Pasadena, California 91103

This report contains information prepared by RCA Corporation under JPL subcontract. Its content is not necessarily endorsed by the Jet Propulsion Laboratory, California Institute of Technology, the National Aeronautics and Space Administration, or the Department of Energy.

DRL Line Item No. 9

DOE/JPL-955825-81/1
Distribution Category UC 63

EVALUATION AND VERIFICATION OF EPITAXIAL PROCESS SEQUENCE FOR SILICON SOLAR-CELL PRODUCTION

D. Redfield
RCA Laboratories
Princeton, New Jersey 08540

QUARTERLY REPORT NO. 1

APRIL 1981

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, under NASA Contract NAS7-100 for the Department of Energy.

The JPL Low-Cost Silicon Solar Array Project is funded by DOE and forms part of the DOE Photovoltaic Conversion Program to initiate a major effort toward the development of low cost solar arrays.

Prepared under Contract No. 955825 for

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
Pasadena, California 91103

PREFACE

This Quarterly Report, prepared by RCA Laboratories, Princeton, NJ 08540, describes the results of work performed from January 27, 1981, to March 31, 1981, in the Energy Systems Research Laboratory, B. F Williams, Acting Director. The Project Scientist is D. Redfield and the Project Supervisor is A. H. Firester, Head, Process and Applications Research. R. V. D'Aiello also participated in the research (cell processing) for this report.

TABLE OF CONTENTS

SECTION I

GOALS AND OBJECTIVES

The goal of this program is to evaluate the applicability of previously developed solar-cell and module processing sequences developed for single-crystal silicon under the sponsorship of the LSA Project, to be used now on lower cost epitaxial silicon wafers. These process sequences have been shown to be of potentially low cost and to perform effectively when applied to the high-quality silicon crystals for which they were developed. The present program is intended to verify the extent to which such process sequences can also perform effectively when applied to lower-cost thin-film solar cells formed by epitaxial deposition of Si on potentially inexpensive substrates of upgraded metallurgical grade (UMG) Si. Therefore, maximum use is being made of process steps developed under the LSA Project, and of epitaxial Si wafer development being performed at RCA Laboratories under the SERI Exploratory Development program.

SECTION II

INTRODUCTION

To achieve the program goals, 28 minimodules will be fabricated and tested, using cells from 600 three-inch-diameter wafers to be processed by the sequence chosen for this purpose. Of these 600 cells, one half are to be made from epitaxially grown layers on potentially low-cost substrates. The other half are to be made from commercial semiconductor-grade (SG), single-crystal silicon wafers that serve as controls. All cell processing is performed on mixed lots containing significant numbers of each of these two types of wafers. After evaluation of the performance of all cells, they will be separated by types and incorporated into modules that will be tested for electrical performance and response to environmental stress. A simplified flow chart displaying this scheme, for quantities representing half of the total to be processed, is shown in Fig. 1.

Documentation of the specifications and procedures of all process steps chosen for this program, and detailed SAMICS cost analyses are to be provided under this program in separate reports bearing those titles. As with all R&D projects, however, there are unavoidable differences between some of the laboratory processes being used to fabricate cells and modules for the present evaluations and the analogous processes as they would take place in a factory at high production rates. In addition, advances in technology may justify substitution of new processes or materials; an example is the projected use of EVA encapsulant in both SAMICS and the process specifications, even though PVB is used in the laboratory modules.

In all cases where uncertainties may exist in specific process steps, the materials or procedures used are consistent with developments occurring under either the LSA program or the Exploratory Development (ED) contract that RCA is conducting for SERI [1]. In this report some information is provided on current work under the ED program that is relevant.

---

1. "Exploratory Development of Thin-Film Polycrystalline Photovoltaic Devices," Solar Energy Research Institute Contract XS-09100-3.

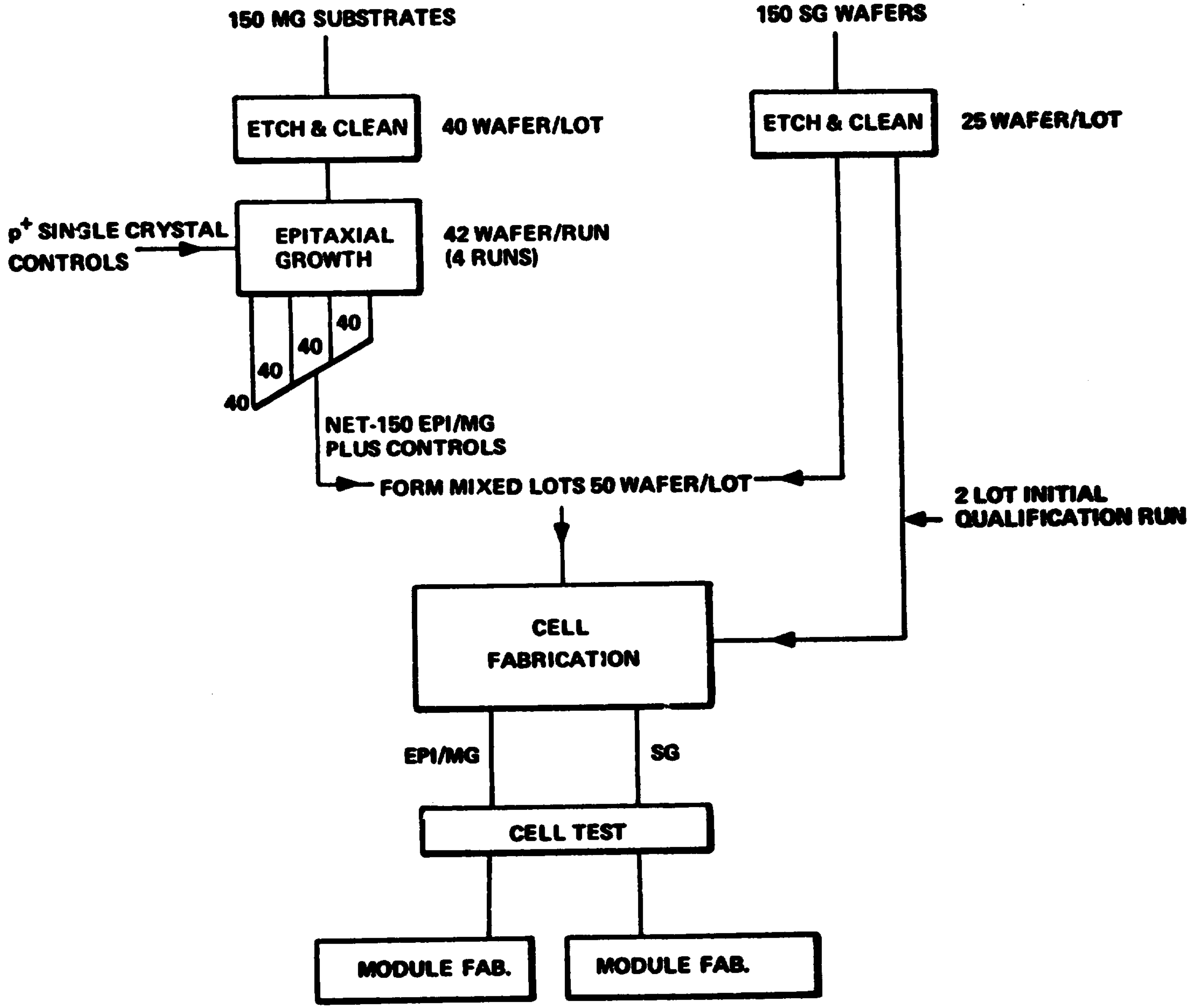

Figure 1. Processing flow chart.

SECTION III

DATA AND RESULTS

Recent progress, present status, and new data are presented by tasks defined in the contract. An overview of the schedule planned for these tasks and the current status of this schedule are presented in the two-page chart at the end of this report.

A. TASK 1 - SILICON SUBSTRATE MATERIALS

1. Epitaxial Substrates

Because low-cost substrates for epitaxial growth of Si are still under development, their properties are not yet thoroughly established. Indeed, there are substantial variations in the properties of substrate materials from different suppliers. RCA has used a variety of such substrates and has chosen for its epitaxial programs materials that are basically upgraded metallurgical grade (UMG) Si (all p-type) as being most promising for meeting both the cost and performance goals of the Exploratory Development contract [1]. The specific type that was selected was the heat-exchanger-method (HEM) Si that is made in large ingots by Crystal Systems, Inc. Therefore, use of that material is planned in this program as well.

For several reasons, however, it was decided during this period to use two types of substrate materials in the present program. One reason was uncertainty regarding the timely availability of enough HEM substrates. A second was the continuing difficulty being experienced in the SERI Exploratory Development program with particulate inclusions in current HEM material. Inclusions occur commonly in wafers obtained to date and have been identified as the cause of low fill factors in large-area cells that cannot exclude them. Lastly, experience with UMG substrates from the Hemlock Semiconductor Corp. (a subsidiary of Dow-Corning Co.) has shown them to be suitable for the present purposes; they are also available to us immediately in sufficient quantity (i.e., 150).

Spectroscopic analysis of the impurity content of these Dow Corning wafers and the electrical resistivities have previously been measured [2]. Although

2. R. V. D'Aiello and P. H. Robinson, "Low-Cost Epitaxial Techniques for Solar-Cell Fabrication," Final Report, SERI/PR-0-8274-4, Nov. 1980, Subcontract No. XS-9-8274.

the impurity content is somewhat variable, the resistivities are quite uniform at 0.01 Ω·cm.

Also now on hand are 50 three-inch-diameter wafers of p^+ CZ silicon for use as control substrates for epitaxial growth. These will be employed in the as-sawed condition to resemble the UMG wafers, which will all be unpolished. The same etching treatment will be used for controls and UMG materials in preparation for epi growth.

2. Epitaxial Growth

Preparation of as-sawed wafers for use as epi substrates has begun. For this purpose 2 mils are etched off each side of all wafers in batches of 25 in an NBK Model SW-100 Etching Apparatus that has just been tested and put into use. The etch takes two minutes in a solution of buffered HF/HNO_3. Following rinsing, the wafers are subjected to a Megasonic cleaning just before placement in the epi reactor.

All epi growths for this program are being done in RCA's high throughput reactor (HTR) which can now process a batch of about 40 wafers at a time with quite good uniformity. On the basis of considerable experience with epitaxially made solar cells, a doping profile such as shown in Fig. 2 was chosen. Not only does such a profile make economical use of the high-quality Si in the epi layer (since that layer is only about 20 μm thick); it also produces naturally a "back-surface field." This field exists as a consequence of the difference in resistivity between the front and the substrate. It can also be easily tailored to provide a wide range of doping gradients in the transition region. Moreover, the high conductivity of the substrates eases problems of making good electrical contact to the back of the cell.

The HTR is now ready for use after receiving several improvements. The entire gas-handling system has been revised with improved components, and the hydrogen gas that is used in quantity as a carrier gas is now supplied from a liquid-hydrogen tank rather than from ordinary cylinders. This enhances the hydrogen purity.

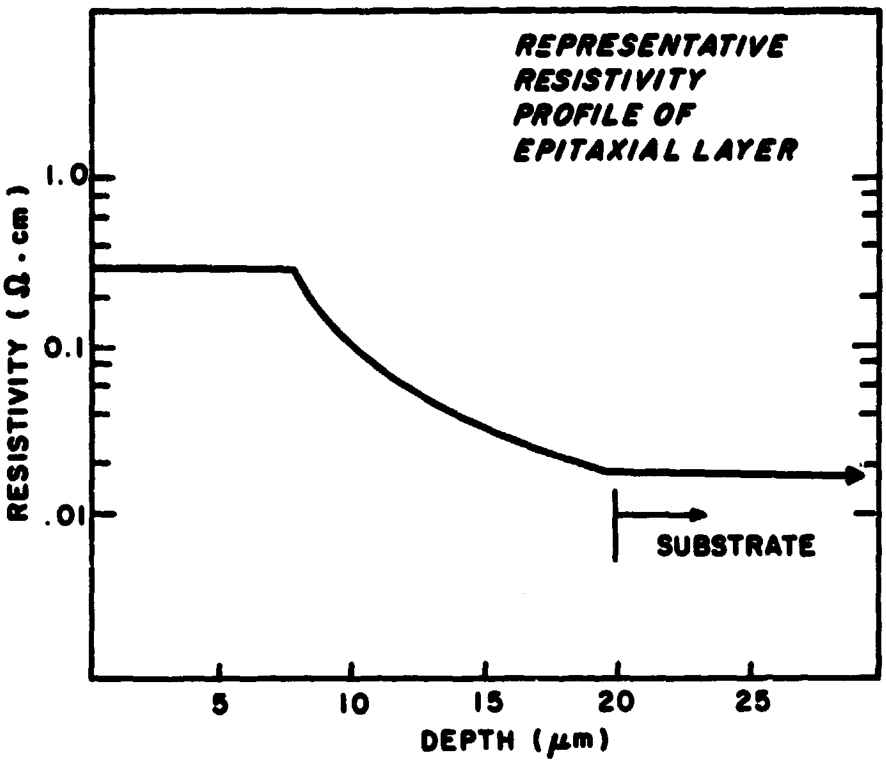

Figure 2. Representative resistivity profile of epitaxial layer.

B. TASK 2 - PROCESS SEQUENCE DETERMINATION

The process sequence chosen for this program is characterized in broad terms by $POCl_3$ junction diffusion, thick-film screen-printed Ag front grid, thick-film aluminum back contact, and sprayed-on antireflection coating. Details have been presented in the Process Development Plan submitted as a separate report. A graphical summary of this sequence appears in Fig. 3.

Of particular importance in this sequence are the screen-printed metallizations. Although promising for cost reduction, this technology is still under development. It is also desirable to eliminate the use of silver eventually, so future changes in this process are possible. The epitaxial cells provide a useful advantage for the back contact, regardless of contacting procedure, because of the high conductivity of all UMG epi substrates. It is generally easier to make good electrical contact to silicon of high conductivity

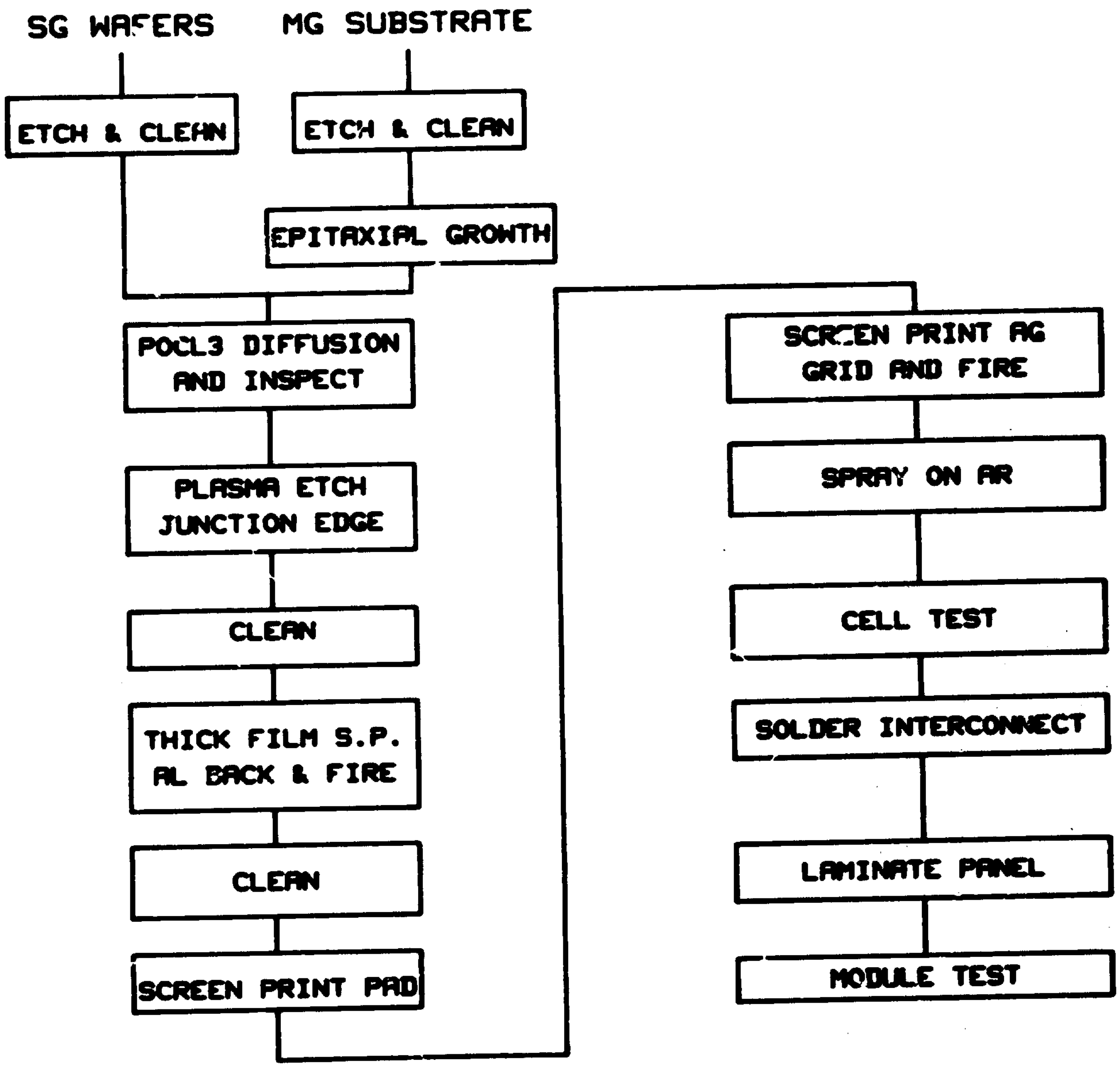

Figure 3. Summary of process sequence.

than of low conductivity. We are attempting to exploit the properties of epi substrates by use of a simple aluminum ink that is fired briefly into the back of epi cells. A final pattern of screen-printed silver covers the Aℓ (after thorough cleaning).

To develop familiarity with this cell-processing sequence in batches of full size, two lots containing only SG wafers (25 in each lot) were processed. These are designated by process lot numbers 01 and 02 even though they contain no epi wafers. The cell-processing sequence was complete for these two lots except that the AR coating was not applied. Thus there is enough information to evaluate the electrical properties of the cells; a good AR coating normally increases the current by a factor of about 1.35, and the efficiency by about 1.4. Of the 50 wafers used in these two lots, 47 complete cells were obtained, for a yield of 94%. In laboratory handling we do not expect to do better than this, although a factory should do considerably better.

Values of V_{oc} and J_{sc} for the cells of these two lots are presented in Table 1. Two significant facts emerge from Table 1: The currents are very good and there is little spread in the values of both V_{oc} and J_{sc}. The mean values and standard deviations for these quantities are given in Table 2.

There were problems with the fill factors that will be described next. First, it is worth noting that the mean values of Table 2 are characteristic of quite good cells. That can be seen by assuming a reasonable fill factor of 0.75 for use with $V_{oc} = 0.56$ and $J_{sc} = 32\ \mathrm{mA/cm^2}$ (including the factor of 1.35 for the effect of an AR coating). Together, these values lead to a mean efficiency of $\eta = 13.4\%$ (at 100 $\mathrm{mW/cm^2}$ irradiance).

The measured fill factors, and therefore the efficiencies, of all cells in lots 01 and 02 were very poor. Additional measurements showed resistive effects in the screen-printed metal contacts. Since these resistive effects diminished somewhat as a consequence of etching in HF, it is clear that part of the problem is in the Ag ink that is used. At present it is uncertain whether the trouble arises at both front and back, or on just one face. It is also not known whether there is too high a resistance at the metal/semiconductor interface. Experiments are under way to answer these questions and to eliminate the problem.

TABLE 1. CURRENTS AND VOLTAGES FOR PROCESS LOTS 1 AND 2

CELL NO	VOC (VOLTS)	JSC (MA/CM**2)
01P01S	.559	23.64
01P02S	.567	24.19
01P05S	.560	24.34
01P06S	.567	24.29
01P07S	.563	23.02
01P08S	.571	21.22
01P09S	.563	21.97
		22.29
01P11S	.561	23.82
01P12S	.558	24.42
01P13S	.558	23.19
01P14S	.567	21.69
01P15S	.552	24.35
01P16S	.562	22.09
01P17S	.560	24.25
01P18S	.562	23.67
01P19S	.557	24.02
01P21S	.555	24.33
01P22S	.557	24.08
01P23S	.553	22.69
01P24S	.558	22.03
01P25S	.557	23.42
02P01S	.565	23.52
02P02S	.562	24.34
02P03S	.561	24.67
02P04S	.561	24.89
02P07S	.555	24.61
02P08S	.559	24.65
02P09S	.559	24.79
02P10S	.559	24.58
02P11S	.559	24.86
02P12S	.562	24.35
02P13S	.558	24.25
02P14S	.558	23.78
02P15S	.570	24.60
02P16S	.554	24.86
02P17S	.558	24.10
02P18S	.561	23.92
02P20S	.557	24.42
02P21S	.554	23.49
02P22S	.547	23.87
02P23S	.556	22.84

TABLE 2. MEAN VALUES AND STANDARD DEVIATIONS σ for V_{oc} and J_{sc} in LOTS 01 AND 02

Parameter	Lot 01	Lot 02
V_{oc}	0.560 V	0.559 V
σ_V	0.005	0.005
J_{sc}	23.3 mA/cm^2	24.3 mA/cm^2
σ_J	1.0	0.55
$1.35xJ_{sc}$ [(a)]	31.5 mA/cm^2	32.8 mA/cm^2

[(a)] The expected current with AR coating is about 1.35 J_{sc}.

C. TASK 3 - PROCESS SPECIFICATIONS

The preliminary set of cell process specifications and procedures has been prepared and submitted in a separate report. These specifications represent the detailed descriptions of the various processes, materials, and procedures for the sequence that is outlined in Fig. 3. All of the specifications are consistent with either the epitaxial cell development by RCA under the ED contract [1] or the various LSA processes that were developed under JPL sponsorship. Because of certain unavoidable differences between laboratory processing as performed in the fabrication of cells under this contract and eventual factory production at high rates, these specifications differ in some details from the currently used processes. One example is the provision of specifications for epitaxial wafers that are 4-inch squares rather than the present 3-inch circles. In addition, recent advances in technology dictated specifications for projected use of EVA encapsulant rather than the PVB now being used.

D. TASK 4 - MINIMODULE DESIGN

Design of the minimodules to be fabricated is complete, and all of the required materials are either on hand or have been ordered. The structure is to be glass/PVB/cell/PVB/Tedlar,* all laminated. For compatibility with JPL

*Reg. trademark for PVS film made by E. I. du Pont de Nemours & Co., Inc., Wilmington, DE.

testing mounts, the modules will have external dimensions to comply with JPL Dwg. No. 10087506, Rev. A as provided to us by JPL. The cells will be series connected as called for in that drawing but no half-cells are planned for use. Also, the number of wafers per module might be less than the 16 shown in that drawing if yields in processing and assembly are too low.

E. TASK 5 - PROCESS AND DESIGN VERIFICATION

Work on this task is to begin later.

F. TASK 6 - COST EVALUATIONS AND PROJECTIONS

An initial SAMICS cost analysis has been prepared and submitted as a separate report. As with the process specifications in Task 3, this analysis is based on the projected factory operation which is, of course, not identical to the present laboratory processes. A brief summary of the principal process steps and their projected costs are presented in Table 3. It can be seen that the projected module price is far below the $700/kWp that is the 1986 goal of this contract. The reason is that the associated Exploratory Development program of SERI has a target date of 1990, by which time it is expected that this epitaxial technology can produce modules at less than $500/kWp.

Two more SAMICS cost analyses will be provided under this program.

TABLE 3. SAMIS COST SUMMARY

Process Step	\$/Wp
HEM Solidification	0.052
Sectioning	0.015
FAST Slice	0.047
Wafer Etch	0.038
Megasonic Clean - 1	0.014
HTR Epi	0.085
$POCl_3$ Deposition	0.007
Junction Plasma Etch	0.007
Megasonic Clean - 2	0.014
Screen Print Al Back	0.008
Screen Print Cu Pad	0.004
Screen Print Ag Grid	0.076
Spray AR	0.007
Cell Test	0.004
Cell Interconnect	0.039
Encapsulation (Springborn)	0.072
Module Test (Motorola)	0.002
Total	0.491

SECTION IV

INTERPRETATIONS OF DATA

At this early state of this contract little interpretation is possible. Results from the RCA Exploratory Development program are currently focusing on the problem of particulate inclusions in the HEM substrates. That problem must be greatly alleviated for large-area solar cells of that material to be successful.

The only processing difficulty encountered to date is that of the screen-printed metals. That may be aggravated on the backside by the fact that the only cells processed so far are lightly doped SG material with no back-surface field. Therefore, the contacting problem on the back is worse than is expected to occur with the epi cells, as these will always have high-conductivity bases. On the front, the present trial wafers had a polished face, a surface condition that is more difficult to contact than are the etched faces that will be used in the future.

SECTION V

TENTATIVE CONCLUSIONS AND RECOMMENDATIONS

Of the processing issues that are current in this period, all appear to be under control except for the screen-printed metals that are producing poor fill factors. Although there are alternative methods for metallization, it is premature now to abandon screen printing. Further evaluations of variations in the metallization and its firing appear to be warranted. One other factor that may play a role, the polished front surface, is also being studied now.

SECTION VI
PROGRAM SCHEDULE

Figure 4 on the next two pages displays the planned schedule of activities on the six tasks of this program with solid lines. Accomplishments to date are shown by the shaded bars above their respective solid lines.

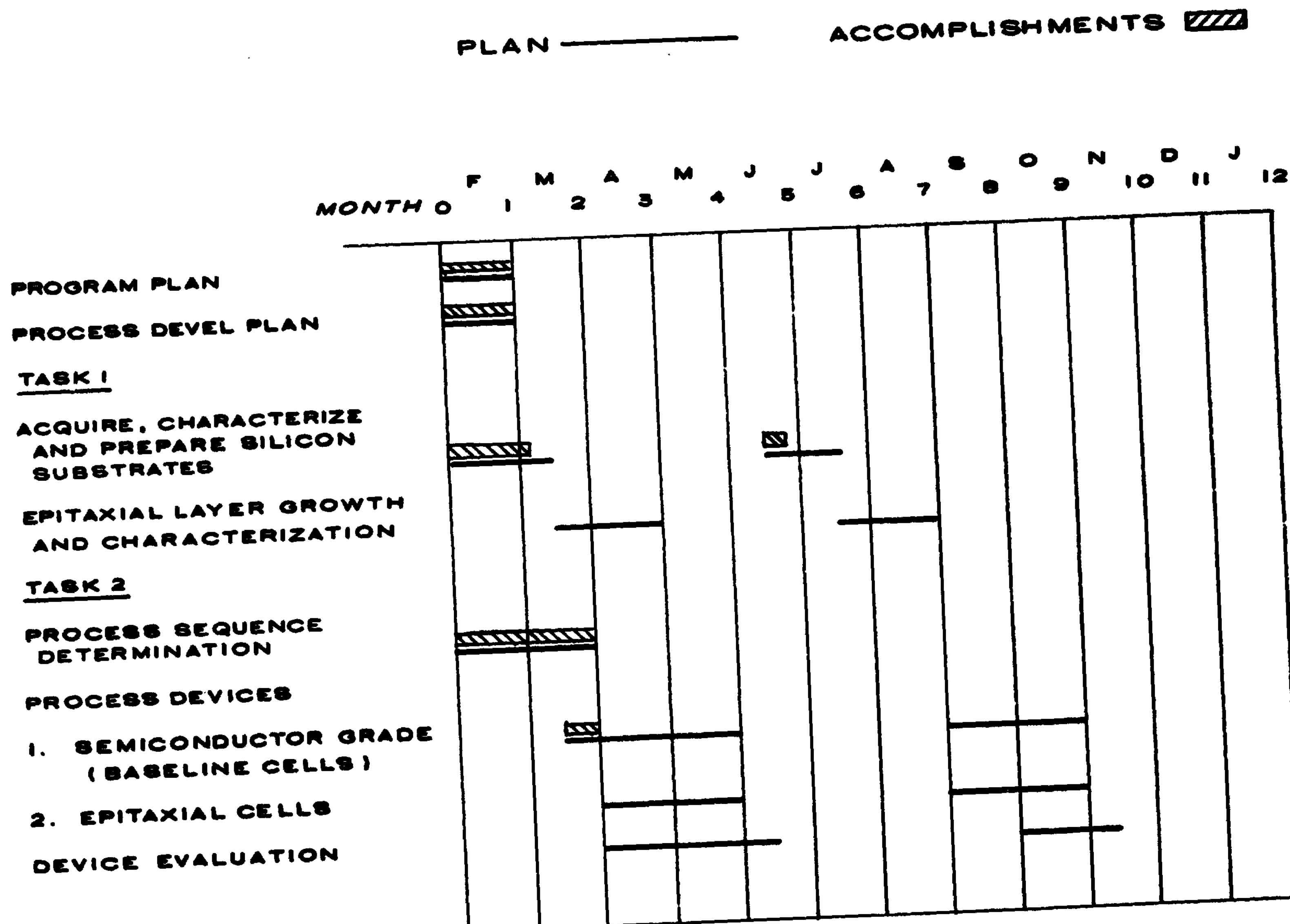

Figure 4. Schedule of accomplishments.

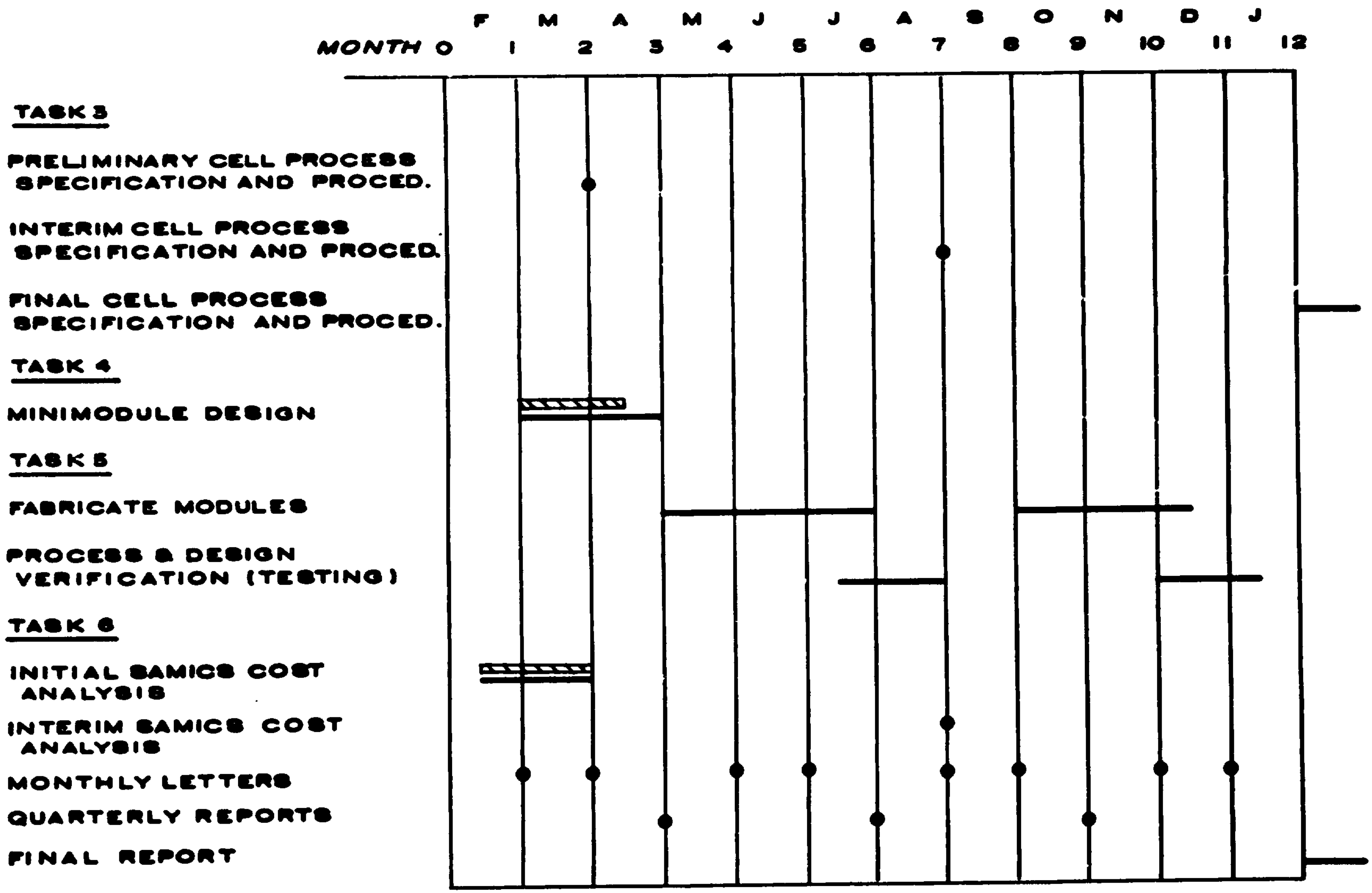

Figure 4. (Continued).